**IN THE SPECIFICATION:**

Amend the paragraph from page 3, line 20 through page 4, line 8, to read:

The ACT type flash memory is so constructed that a control gate 1, an interlayer insulator 2, a floating gate 3 and a tunnel oxide 4 are formed in layers so as to stretch over a drain 6 and a source 7 provided in a substrate (P-type well) 5. It is noted that the drain 6 and the source 7 have different donor concentrations. Then, in the program operation in which electrons are pulled out from the floating gate 3, a negative voltage of -8 V is applied to the control gate 1 and a positive voltage of +5 V is applied to the drain 6 so that the source 7 is put into a floating state, where the electrons are pulled out from the floating gate 3 by the FN tunneling phenomenon. As a result, the threshold of the memory cell to be programmed is lowered to about 1.5 V.

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Amend the paragraph beginning on page 4, line 9, to read:

Also, in the erase operation in which electrons are injected into the floating gate 3, a positive voltage of +10 V is applied to the control gate 1, a negative voltage of -8 V is applied to the source 7 and a negative voltage of -8 V is applied to the drain 6, where the electrons are injected into the floating gate 3 by the FN tunneling phenomenon. As a result, the threshold of the cell to be erased is increased so as to rise to about 4 V or more. Like this, the ACT type flash memory is an FN-FN type flash memory.

**IN THE CLAIMS:**

Cancel claim 1 without prejudice or disclaimer.

Amend claim 2 to read:

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2. (Amended) An erase method for a nonvolatile semiconductor storage device in which floating gate field effect transistors each having a control gate, a floating gate, a drain and

a source and being electrically information programmable and erasable are arrayed in a matrix shape on a substrate or well, and which comprises a plurality of row lines connected to the control gate of each floating gate field effect transistors arrayed along a row direction, and a plurality of column lines connected to the drain and source of each floating gate field effect transistors arrayed along a column direction, the method comprising:

using the Fowler-Nordheim tunneling phenomenon for both programming and erasing; and

B2 cont

for erasing, applying a negative first voltage to the substrate or well and applying a positive voltage to select row lines, while applying a negative second voltage to non-select row lines, wherein

the negative second voltage has an absolute value smaller than an absolute value of the negative first voltage.